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WIGGIN AND DANA LLP
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EXAMINER	
YEUNG LOPEZ, FEIFEI	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/561,381	ISLAM ET AL.	
	Examiner	Art Unit	
	Feifei Yeung-Lopez	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *13-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bayan et al (US Patent 6,664,615 B1), in view of Brodsky (US Patent 6,670,222 B1).

4. Regarding claim 1, Bayan teach that a package for encasing at least one semiconductor device (column 8, lines 21-24), comprising: a lead frame having opposing first and second end (top surface of element 600 in fig 7b), said first ends of said lead frame ((element 750 in fig 7b) terminating in an array of lands adapted to be bonded to external circuitry (PCB 790 in fig. 7b) and said second end is directly electrically interconnected to input/output pad (element 710 in fig. 7b) on said at least one semiconductor device; routing circuits (element 600 in fig. 7b) electrically

interconnecting said array of lands (14) and said chip attach site; a first molding compound (dielectric 690) disposed between individual lands of said array of lands; and a second molding compound (encapsulant 725 in fig. 7b) encapsulating said at least one semiconductor device, said chip attach site and said routing circuits.

5. However, Bayan do not teach that the chip attach site is an array of chip attach sites, nor do Bayan teach more than one input/output pad.

6. In the same field of endeavor, Brodsky teaches that indentations on an upper surface of die attachment pad 52 (analogous to element 600 in the primary reference in fig. 7b) for the benefit of enhancing attachment (column 8, lines 21-24 and lines 56-61).

7. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to make indentations on an upper surface of lead frame 600 in fig. 7b in Bayan's package to realize an array of chip attach sites for the benefit of enhancing attachment. It would also have been obvious to one of ordinary skill in the art at the time of the invention to make indentations on an upper surface of die attach material 710 of Bayan's package to realize more than one input/output pad for the benefit of enhancing attachment of the input/output pad to the semiconductor die.

8. Claims 2-5 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bayan et al (US Patent 6,664,615 B1), in view of Brodsky (US Patent 6,670,222 B1) as applied in claim 1 above, further in view of Hsu et al (US Patent 6,380,002 B2).

9. Regarding claim 2, the previous combination remains as applied in claim 1.

10. However, the previous combination does not teach that said lead frame and said routing circuits are elements of a single electrically conductive substrate.

11. In the same field of endeavor, Hsu teach a lead frame (the metal mentioned in column 2, lines 45-52) having an array of lands (chip connection pads 220c in fig. 7) adapted to be bonded to external circuitry, an array of chip attach sites (220d), and routing circuits (conductive traces 220e) electrically interconnecting the array of lands and the array of chip attach sites, made from elements of a single electrically conductive substrate (the metal) for the benefit of reducing delamination (column 1, lines 59-65).

12. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to make said lead frame and said routing circuits elements of a single electrically conductive substrate for the benefit of reducing delamination.

13. Regarding claim 3, the previous combination remains as applied in claim 1.

14. However, the previous combination does not teach that said single electrically conductive substrate is copper or a copper-base alloy.

15. Hsu teach a single electrically conductive substrate is copper (claim 3).

16. Regarding claim 4, the previous combination remains as applied in claim 1.

17. Furthermore, Bayan teach that the package of claim 2 wherein a first perimeter defined by said array of lands does not exceed a second perimeter defined by said at least one semiconductor device (see fig. 7b).

18. Regarding claim 5, the previous combination remains as applied in claim 1.

19. Furthermore, Bayan teach that the package of claim 4 being a chip scale package. Note that Bayan teach a single-chip package (fig. 7b), thus it's a chip scale package.

20. Regarding claim 9, the previous combination remains as applied in claim 1.

21. Furthermore, Bayan teach that the package of anyone of claim 2 further including a die pad (the pad boning the wire to the die on top of the die in fig. 7b) for bonding one of said at least one semiconductor devices, said die pad being monolithic with said lead frame. Note that the pad is bonded to the lead frame, thus it's monolithic with said lead frame.

22. Regarding claim 10, the previous combination remains as applied in claim 1.

23. Furthermore, Bayan teach that the package of anyone of claim 2 further including bond sites (the areas of lead frame 600 where the wires 680 are attached in fig. 7b) for bonding a passive device (the pads that bond the wires in fig. 7b), said bond sites being monolithic with said lead frame.

24. Regarding claim 11, the previous combination remains as applied in claim 1.

25. Furthermore, Bayan teach that the package of claim 2 wherein said array of lands and said first molding compound are coplanar (fig. 7b).

26. Regarding claim 12, the previous combination remains as applied in claim 1.

27. Furthermore, Bayan teach that the package of claim 2 wherein said array of lands extend beyond said first molding compound. Note that the lands (elements 750) are thicker than the first molding compound (dielectric 690), and they extend beyond the molding compound on the bottom (fig 7b).

28. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bayan et al (US Patent 6,664,615 B1), in view of Brodsky (US Patent 6,670,222 B1) , further in view of Hsu et al (US Patent 6,380,002 B2) as applied to claim 2 above, and still further in view of Shimanuki et al (PG Pub 2002/0168796 A1).

29. Regarding claim 6, the previous combination remains as applied in claim 2.

30. The previous combination teaches a distance between said at least one semiconductor device and said routing circuits is filled with said second molding compound. Note that Bayan teach that die 650, bonding wires, and gaps between leads in patterned lead frame 600 are filled with molded plastic (second molding compound, column 7, lines 38-41).

31. Further, Brodsky teaches that the depth of the indentations 51 (fig. 4) is in the range of submicron to about 15 microns (column 9, lines 1-6).

32. However, the previous combination does not teach a distance between said at least one semiconductor device and said routing circuits is at least 75 microns.

33. In the same field of endeavor, Shimanuki teach an array of chip attach sites has a vertical dimension of 0.5mm or 500 microns (paragraph [0187].

34. Note that discovery of an optimum range is well within the level of ordinary skill in the art, and such ranges will not support patentability unless there is evidence of its criticality. In re Aler, 220 F.2d 454.456.

35. Regarding claim 7, the previous combination remains as applied in claim 2.

36. Brodsky teaches that the depth of the indentations 51 (fig. 4) is in the range of submicron to about 15 microns (column 9, lines 1-6).

37. In the same field of endeavor, Shimanuki teach an array of chip attach sites has a vertical dimension of 0.5mm or 500 microns (paragraph [0187].

38. Note that discovery of an optimum range is well within the level of ordinary skill in the art, and such ranges will not support patentability unless there is evidence of its criticality. In re Aler, 220 F.2d 454.456.

39. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bayan et al (US Patent 6,664,615 B1), in view of Brodsky (US Patent 6,670,222 B1), further in view of Hsu et al (US Patent 6,380,002 B2) as applied to claim 2 above, and still further in view Hauer et al (US Patent 5,600,741).

40. Regarding claim 8, the previous combination remains as applied in claim 2.

41. Moreover, Hsu teach a single electrically conductive substrate (a metal mentioned in column 2, lines 45-52) forming a lead frame having an array of lands (220d in fig. 7).

42. However, the previous combination does not teach a heat sink that is a single electrically conductive substrate with said lead frame and coplanar with said array of lands.

43. In the same field of endeavor, Hauer teach a substrate having a land (area of the substrate contacting the laser 50 in fig. 3), where the substrate is simultaneously being

used as heat sink (column 4, lines 61-66) for the benefit of reducing the size of the device in fig. 3 as a whole, comparing to adding an additional heat sink to the device. Note that when Hsu's lead frame is simultaneously used as a heat sink, the heat sink would be coplanar with said array of lands.

44. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a heat sink that is a single electrically conductive substrate with said lead frame and coplanar with said array of lands for the benefit of reducing the size of the device.

Response to Arguments

1. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Feifei Yeung-Lopez whose telephone number is 571-270-1882. The examiner can normally be reached on 7:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FYL

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PRIMARY EXAMINER